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Docket No.: 42390P10576

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jason Ross, et al.

Application No.: 09/822,715

Filed: March 30, 2001

For: BURIED INTERSIGNAL CAPACITANCE

Examiner: Quynh-Nhu H.

Art Group: 2841

AMENDMENT AND RESPONSE TO THE OFFICE ACTION

Assistant Commissioner for Patents
Washington, DC 20231-9998

Sir:

In response to the outstanding Office Action mailed October 16, 2001, please amend the above-identified Application as follows:

IN THE DRAWINGS

Enclosed herewith is amended Figure 2 in which the proposed changes are made in red ink and new Figures 2B and 2C. Applicant respectfully requests the Examiner to accept amended Figure 2 and new Figures 2B and 2C because they correct informalities pointed out by the Examiner.

IN THE SPECIFICATION

Please replace the paragraph beginning on page 3, line 6 with the following paragraphs:

A1

Figure 2A is a diagram illustrating a computer-aided design (CAD) of buried intersignal capacitance mode compensation (BICMC) on a PCB according to one embodiment of the invention.

Figure 2B is a diagram illustrating a CAD of a first layer of the PCB shown in Figure 2A.

Figure 2C is a diagram illustrating a CAD of a second layer of the PCB shown in Figure 2A.

Please replace the paragraph beginning on page 4, line 11 with the following paragraph:

Figure 1 is a diagram illustrating a parallel plate capacitor 100 in which one embodiment of the invention can be practiced.

Please replace the paragraph beginning on page 5, line 10 with the following paragraph:

A2

Figures 2A-2C are an illustration of a top view computer-aided design (CAD) layout of the buried intersignal capacitance mode compensation (BICMC) on a printed circuit board (PCB) 200 according to one embodiment of the invention.

Please replace the paragraph beginning on page 6, line1 with the following paragraph:

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Buried Intersignal Capacitance (BIC) is a method of arranging traces in a PCB that allows the board designer to create a specified amount of capacitance between signals. The BIC is formed by creating parallel plates on adjacent layers of a circuit board while preserving the existing circuit board structure. The BIC is used in mode compensation to improve signal quality in the PCB. One of the effective placements of the mode compensating capacitor is between adjacent signal traces at the receiver end of the trace. Placing the mode compensation capacitor at the driver end of the two adjacent signal traces is an alternative way to improve signal quality in the PCB. Mode compensation counteracts the tendency of odd-mode crosstalk to travel faster than even-mode crosstalk through a microstrip transmission line. Even-mode crosstalk occurs when a signal line changes its

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level in one direction and an adjacent signal line changes its level in the same direction (i.e., the signal line is changed from low to high and the adjacent signal line is also changed from low to high). Odd-mode crosstalk occurs when a signal line changes its level in one direction and the adjacent signal line changes its level in the opposite direction (i.e., the signal line is changed from low to high and the adjacent signal line is changed from high to low).

Please replace the paragraph beginning on page 9, line 16 with the following paragraph:

A4

A signal layer 301A includes signal paths 302A and 302B having vias 303A and 303B, respectively. The signal paths 302A and 302B carry signals between devices on the PCB 200. The two signal paths 302A and 302B may be horizontally adjacent to one another and on the same plane (i.e., signal plane) or may be vertically adjacent to one another on two different but adjacent planes. The via 303A as shown on the signal layer 301A is used to interconnect signal path 302A on the signal layer 301A to the signal path 302A on the next layer 301B. In other words, the signal path 302A extends down from the via 303A to beneath the signal path 302B, turns, and follows parallel to the signal path 302B.

Please replace the paragraph beginning on page 10, line 1 with the following paragraph:

A5

A buried interconnect capacitance (as discussed in reference to Figures 2A-2C) is created between the signal path 302B of the signal layer 301A and the signal path 302A of the next layer 301B. These two paths run immediately above/below each other and are separated by a dielectric layers. The size of the capacitance can be controlled by adjusting the distance between the signal path 302B on signal layer 301A and the signal path 302 on the adjacent routing layer 301B.

IN THE CLAIMS

Following is a complete set of claims as amended with this Response. This complete set of claims includes amended claims 1, 8, and 15 and new claims 22-40.

1. (Amended) An apparatus comprising:

a first signal path connected to a first plane via a plated hole, the first signal path on a second plane;

a first metal flood connected to the plated hole to form a first plate, the first metal flood on the first plane;

a second signal path on the second plane; and

a second metal flood connected to the second signal path to form a second plate above the first plate, the second plate on the second plane.

2. The apparatus of claim 1 wherein the first and second plates form a capacitance.

3. The apparatus of claim 1 wherein the first plate is connected at one of a first receiver end and a first driver end of the first signal path.

4. The apparatus of claim 1 wherein the second plate is connected at one of a second receiver end and a second driver end of the second signal path.

5. The apparatus of claim 4 wherein the first and second signal paths are adjacent to each other.

6. The apparatus of claim 1 wherein the first plane is one of a ground plane and a power plane.

7. The apparatus of claim 6 wherein the first metal flood is an isolated area in the first plane.

8. (Amended) A method comprising:

connecting a first signal path to a first plane via a plated hole, the first signal path on a second plane;

forming a first plate by connecting a first metal flood to the plated hole, the first metal flood on the first plane; and

connecting a second metal flood to a second signal path on the second plane to form a second plate above the first plate.

9. The method of claim 8 wherein the first and second plates form a capacitance.

10. The method of claim 8 wherein the first plate is connected at one of a first receiver end and a first driver end of the first signal path.

11. The method of claim 8 wherein the second plate is connected at one of a second receiver end and a second driver end of the second signal path.

12. The method of claim 11 wherein the first and second signal paths are adjacent to each other.

13. The method of claim 8 wherein the first plane is one of a ground plane and a power plane.

14. The method of claim 13 wherein the first metal flood is an isolated area in the first plane.

15. (Amended) A system comprising:

a through hole component to hold a component that is mounted on a board, the through hole component having one of a first receiver end and a first driver end; a signal carrying module coupled to the through hole component to carry signal, the signal carrying module comprising:

a first signal path connected to a first plane via a plated hole, the first signal path on a second plane;

a first metal flood connected to the plated hole to form a first plate, the first metal flood on the first plane;

a second signal path on the second plane; and

a second metal flood connected to the second signal path to form a second plate above the first plate, the second plate on the second plane.

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16. The system of claim 15 wherein the first and second plates form a capacitance.

17. The system of claim 15 wherein the first plate is connected at one of the first receiver end and the first driver end of the first signal path.

18. The system of claim 15 wherein the second plate is connected at one of a second receiver end and a second driver end of the second signal path.

19. The system of claim 18 wherein the first and second signal paths are adjacent to each other.

20. The system of claim 15 wherein the first plane is one of a ground plane and a power plane.

21. The system of claim 20 wherein the first metal flood is an isolated area in the first plane.

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22. (New) The apparatus of claim 1 further comprising:
a dielectric layer between the first plate and the second plate.

23. (New) The apparatus of claim 2 wherein the capacitance is a buried intersignal capacitance.

24. (New) The method of claim 8 further comprising:
forming a dielectric layer between the first plate and the second plate.

25. (New) The method of cliam 9 wherein the capacitance is a buried intersignal capacitance.

26. (New) The system of claim 15 further comprising:

forming a dielectric layer between the first plate and the second plate.

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27. (New) The system of claim 16 wherein the capacitance is a buried intersignal capacitance.

28. (New) An apparatus comprising:

a printed circuit board;

a first transmission line on a first layer of the printed circuit board;

a second transmission line on the first layer of the printed circuit board; and

a capacitor connected to the first transmission line and the second transmission line, the capacitor comprising:

a first plate connected to the first transmission line by a plated hole, the first plate on a second layer of the printed circuit board;

a second plate connected to the second transmission line, the second plate on the first layer of the printed circuit board; and

a dielectric layer between the first plate and the second plate, the dielectric layer between the first layer of the printed circuit board and the second layer of the printed circuit board.

29. (New) The apparatus of claim 28 wherein the first plate is above the second plate.

30. (New) The apparatus of claim 28 wherein the second plate is above the first plate.

31. (New) The apparatus of claim 28 wherein the capacitor is a buried intersignal capacitor.

32. (New) The apparatus of claim 31 wherein the buried intersignal capacitor mode compensates to improve signal quality in the printed circuit board.

33. (New) The apparatus of claim 32 wherein the buried intersignal capacitor matches the propagation speed of odd-mode switch signals with the propagation speed of even-mode switch signals.

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34. (New) The apparatus of claim 28 wherein the first layer of the printed circuit board and the second layer of the printed circuit board are adjacent layers.

35. (New) The apparatus of claim 28 wherein the first plate is connected at a first receiver end of the first transmission line and the second plate is connected a second receiver end of the second transmission line.

36. (New) The apparatus of claim 28 wherein the first plate is connected at a first driver end of the first transmission line and the second plate is connected at a second driver end of the second transmission end.

37. (New) The apparatus of claim 28 wherein the first transmission line is adjacent to the second transmission line.

38. (New) The apparatus of claim 28 wherein the first transmission line is inductively coupled to the second transmission line.

39. (New) The apparatus of claim 28 wherein the first transmission line and/or second transmission line are routed as microstrips.

40. (New) The apparatus of claim 28 wherein first transmission line and the second transmission line are routed on surface layers of the printed circuit board.

REMARKS

This Amendment is in response to the Office Action mailed October 16, 2001. In the Office Action, the Examiner objected to the (i) drawings and rejected (i) claims 1-21 under 35 U.S.C. §112, second paragraph, (ii) claims 1-21 under 35 U.S.C. §102(e).

I. DRAWINGS

In the Office Action, the drawings were objected to as failing to comply with 37 CFR 1.84 (p)(5) because they do not include several reference signs mentioned in the description. Applicant respectfully requests postponement in submitting the formal drawings until the pending claims have been allowed. Moreover, Applicant submits herewith amended Figure 2 in which the proposed changes are made in red ink and further submits new Figures 2B and 2C. As suggested by the Examiner, Figure 2 has been amended to include the following reference signs in the description: "element 211_M", "element 212_M; and "element 213_M." Furthermore, as requested by the Examiner, new Figures 2B and 2C are provided to illustrate the two separate layers of the PCB (200). Applicant respectfully requests acceptance of amended Figure 2 and new Figures 2B and 2C because no substantive new matter has been added. A separate letter regarding these proposed changes is being sent to the draftsperson as set forth in MPEP §602.02(r). Applicant requests that he be allowed to postpone submitting final formal drawings until the claims have been allowed.

II. SPECIFICATION

The specification has been amended to correct informalities and to describe new Figures 2B and 2C. Applicant respectfully requests acceptance of the amended specification because no substantive new matter has been added.

III. CLAIMS

REJECTION UNDER 35 U.S.C. § 112

The Examiner rejected claims 1-21 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

The Office Action states that the specification and drawings describe a "first signal path is [on the] same plane surface with a first plane." It is respectfully submitted that the specification and drawings do not describe such a configuration in the embodiment illustrated in Figure 2 of the present application. In accordance with this embodiment, the first signal path (215_2) is not on the first plane which includes a lower plate (212_1) (see Figure 2). In fact, the first signal path is on a second plane which includes a second plate (211_1). As such, claims 1, 8, and 15 correctly describe the embodiment illustrated in Figure 2 of the present application. It is submitted that the indefiniteness rejection of claims 1-21 be removed.

REJECTION UNDER 35 U.S.C. § 102(e)

The Examiner rejected claims 1-21 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,175,088 issued to *Saccocio*.

In response thereto, claims 1, 8, and 15 have been amended and new claims 22-24 have been added. Accordingly, claims 1-24 are now pending. Following is a discussion of the patentability of each of the pending claims.

Independent Claim 1

Claim 1 recites an apparatus with a first signal path connected to a first plane via a plate hole. The first signal path is on a second plane. A first metal flood is connected to the

plated hole to form a first plate. The first metal flood is on the first plane. A second signal path is on a second plane. A second metal flood is connected to the second signal path to form a second plate above the first plate. The second plate is on the second plane.

In accordance with the Office Action, the *Saccocio* reference discloses a multi-layer printed-wiring board (100) having a first signal path (201) connected to a first plane (102) via a plated hole (110). A first metal flood (205 or 206) is connected to the plated hole to form a first **plane**. A second signal path (206) is on a second plane (102). A second metal flood (204 or 205) is connected to the second signal path (206) to form a second plate above the first **plane**. It is noted that Figures 1 and 2 of the *Saccocio* reference do not disclose a second metal flood (204 or 205) which forms a second plate **above** the first plane (102) as suggested by the Office Action. To the contrary, the *Saccocio* reference discloses a second metal flood (204 or 205) which forms a second plate that is on the same plane as the first plane (102). Furthermore, claim 1 recites a first metal flood connected to the plated hole to form a first **plate** and further recites a second metal flood connected to the second signal path to form a second **plate**. The Office Action states the word "plane" instead of "plate" when describing the elements of the multi-layer printed-wiring board of the *Saccocio* reference.

Furthermore, the *Saccocio* reference does not disclose a first signal path on a second plane and a second signal path on the second plane as recited in claim 1 of the present application. In other words, the first signal path and the second signal path are on the same plane. In the *Saccocio* reference, the first signal path (201) is on a surface layer plane (101) and the second signal path (206) is on the second plane (102).

Accordingly, it is respectfully submitted that claim 1 is in condition for allowance.

Dependent Claims 2-7 and 22

Claims 2-7 and 22 depend from claim 1 are similarly patentable. Accordingly, it is respectfully submitted that these claims are in condition for allowance.

Independent Claim 8

Claims describes a method comprising the following: connecting a first signal path to a first plane via a plated hole, the first signal path on a second plane; forming a first plate by connecting a first metal flood to the plated hole, the first metal flood on the first plane; and connecting a second metal flood to a second signal path on the second plane to form a second plate above the first plate.

For at least the same reasons discussed above in reference to claim 1, it is respectfully submitted that claim 8 is in condition for allowance.

Dependent Claims 9-14 and 23

Claims 9-14 and 23 depend from claim 8 and are similarly patentable. Accordingly, it is respectfully submitted that these claims are in condition for allowance.

Independent Claim 15

Claims describes a system having a through hole component that is mounted on a board. The through hole component has a first receiver end and a first driver end. A signal carrying module is coupled to the through hole component to carry signal. The signal carrying module has a first signal path connected to a first plane via a plated hole. The first signal path is on a second plane. A first metal flood is connected to the plated hole to form a first plate. The first metal flood is on the first plane. A second signal path is on the second plane. A second metal flood is connected to the second signal path to form a second plate above the first plate. The second plate is on the second plane.

For at least the same reasons discussed above in reference to claim 1, it is respectfully submitted that claim 15 is in condition for allowance.

Dependent Claims 16-21 and 24

Claims 16-21 and 24 depend from claim 15 and are similarly patentable. Accordingly, it is respectfully submitted that these claims are in condition for allowance.

CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that all pending claims are in condition for allowance, and such action is respectfully solicited.

Respectfully submitted,

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Dated: December 21, 2001

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: December 21, 2001.

Laura Robles — *Date* 12/21/01